

U.S. Department of Commerce, Patent and Trademark				Atty. Docket No.		Application No.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				SNDK.352US0		10/799,060	
				Applicant(s)			
(Use several sheets if necessary)				Jeffrey Lutze et al.			
				Filing Date		Group	
				March 12, 2004		2818	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
MH	001	5,043,940	8/1991	Harari			
	002	5,070,032	12/1991	Yuan			
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	023	5,654,217	8/1997	Yuan			
	024	5,661,053	8/1997	Yuan			
✓	025	5,677,872	10/1997	Samachisa			
Examiner	Date Considered		08/11/05				
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<i>mt</i>	026	5,712,179	1/1998	Yuan	<del>_____</del>	<del>_____</del>	
	027	5,712,180	Jan. 27, 1998	Guterman et al.	<del>_____</del>	<del>_____</del>	
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	030	5,786,988	7/1998	Harari	<del>_____</del>	<del>_____</del>	
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	042	6,208,545B1	3/2001	Leedy	<del>_____</del>	<del>_____</del>	
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	049	6,417,538	7/2002	Choi	<del>_____</del>	<del>_____</del>	
	050	6,455,440	Sep. 24, 2002	Jeng Pei-Ren	<del>_____</del>	<del>_____</del>	
	051	6,512,263	1/2003	Yuan	<del>_____</del>	<del>_____</del>	
	052	6,529,410	3/2003	Han et al.	<del>_____</del>	<del>_____</del>	
	053	6,562,682	May 13, 2003	Chen Ming-Shang et al.	<del>_____</del>	<del>_____</del>	
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Examiner <i>Chen</i>			Date Considered <i>8/11/05</i>				
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							Translation
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
MT	062	Aritome, Seiichi, "Advanced Flash Memory Technology and Trends for File Storage Application," IEDM Technical Digest, International Electronic Devices Meeting, IEEE, San Francisco, California, December 10-13, 2000, pp 33.1.1-33.1.4.					
	063	Chan, et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," <i>IEEE Electron Device Letters</i> , Vol. EDL-8, No. 3, March 1987, pp. 93-95.					
	064	DiMaria et al., "Electrically-alterable read-only-memory using Si-rich SiO <sub>2</sub> injectors and a floating polycrystalline silicon storage layer," <i>J. Appl. Phys.</i> 52(7), July 1981, pp. 4825-4842.					
	065	Eitan et al., "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," <i>IEEE Electron Device Letters</i> , Vol. 21, No. 11, November 2000, pp. 543-545.					
	066	Hori et al., "A MOSFET with Si-implanted Gate-SiO <sub>2</sub> Insulator for Nonvolatile Memory Applications," IEDM 92, April 1992, pp. 469-472.					
	067	Lee, Jae-Duk, et al., "Effects of Parasitic Capacitance on NAND Flash Memory Cell Operation," Non-Volatile Semiconductor Memory Workshop, IEEE, Monterey, California, August 12-16, 2001, pp. 90-92.					
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		Document	Date	Country	Class	Subclass	Yes	No
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44	068	Nozaki et al., "A 1-Mb EEPROM with MONOS Memory Cell for Semiconductor Disk Application," <i>IEEE Journal of Solid State Circuits</i> , Vol. 26, No. 4, April 1991, pp. 497-501.						
44	069	Takeuchi, Y., et al., "A Self-Aligned STI Process Integration for Low Cost and Highly Reliable 1Gbit Flash Memories," 1998 Symposium on VLSI Technology; Digest of Technical Papers, IEEE, Honolulu, Hawaii, June 9-11, 1998, pp. 102-103.						
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